REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 3, 4, 6-8, 11, 12 and 18-20 are presently pending in this application, Claim 1 having been amended by the present amendment.

In the outstanding Office Action, Claims 1-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sakamoto et al. (U.S. Patent 6,687,985) in view of Jones et al. (U.S. Patent 5,541,450); and Claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sakamoto et al. in view of Jones et al. and Londa (U.S. Patent 5,963,430).

Turning now to the merits, Applicants' invention is directed to a multilayered printed circuit board having an opening for accommodating an IC component, and having a structure for irradiating heat from the IC component. In order to expedite issuance of a patent in this case, Applicants have amended Claim 1 to clarify the heat irradiating structure in relation to the IC component.

Specifically, amended Claim recites Claim 1 a multi-layer printed wiring board including a first substrate having an opening and having a plurality of external terminals positioned to be connected to a package substrate, and a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board. The second substrate has a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion. Also recited is an IC component having a terminal side including a plurality of terminals, and a non-terminal side which is opposite to the terminal side. The IC component is loaded in the opening of the first substrate such that the non-terminal side of the IC component contacts the metallic layer portion and the terminals of the IC component face outward of the opening in the first substrate. The IC component is

accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component.

Thus, Claim 1 is amended to clarify that the ***IC component has a terminal side and a non-terminal side,*** and that the IC component is loaded in the opening of the first substrate such that ***the non-terminal side of the IC component contacts the metallic layer portion and the terminals of the IC component face outward of the opening in the first substrate.*** An example of this configuration is shown in Figs. 1 and 2 of Applicants specification. As seen in these Figures, the metal layer 28a is provided in contact with the non-terminal side of the IC component 70, and also contacts the non-through holes 18a in the second substrate, which irradiate heat away from the IC 70. Thus, heat generated by the IC component is effectively radiated to and removed through the metallic layer portion and the non-through holes, thereby preventing heat damage caused by the IC component.

In contrast, Sakamoto et al. shows a carrier board 16 is set in a cavity 15 of a mother board 11 and electrically connected to the mother board 11. As seen in Fig. 1 of Sakamoto et al., the carrier board includes electrodes 21 provided on a first side for connecting to the electrodes 22 of the mother board, and also includes lands 17 and wiring patterns 18 provided on an opposing side facing outward of the opening in the mother board. That is, carrier board has electrical terminals on both sides thereof.

Thus, even if the carrier board 16 is considered to be an "IC component," this component cannot provide the feature of an IC component having a terminal side including a plurality of terminals, and a non-terminal side which is opposite to the terminal side, the IC component being loaded in the opening of the first substrate such that the non-terminal side of the IC component contacts the metallic layer portion and the terminals of the IC component face outward of the opening in the first substrate, as now required by amended Claim 1.

Moreover, there is no indication in Sakamoto et al. that the via-hole conductors 14 are configured to irradiate heat from the carrier board. As such, Sakamoto et al. also fails to disclose that the carrier board is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the carrier board, as also required by Claim 1. Indeed, one would not expect the carrier board 16 to generate the substantial heat of an IC component or even need to remove heat therefrom.

Jones et al. discloses a perimeter BGA package or structure 30 in which a semiconductor die 18 is set in an opening 33 of a substrate 31. As seen in the figures of Jones et al., the die is attached by way of an attach pad 36 to a support 32. However, there are no "non-through holes" connected to the pad 36 for irradiating heat from the die 36. In this regard, Applicants submit that Jones et al. does not provide any structure (other than the support 32 itself) in contact with the non terminal side of the die 18. Thus, Jones et al. cannot correct the deficiencies of Sakamoto et al.

Still further, one of ordinary skill in the art would not find it obvious to combine the die 18 and die attach pad 36 within the opening of the motherboard in Sakamoto et al. as noted above, the opening in Sakamoto et al. includes contacts 22 for accommodating the terminals of the carrier. Thus, the attach pad 36 (assuming that it is made of metal) would short the contacts 22 and render the motherboard inoperable.

Therefore, it is respectfully submitted that the structure recited in Claim 1 is believed to be distinguishable from both Sakamoto et al. and Jones et al., and because Sakamoto et al. and Jones et al. fail to disclose the second substrate as recited in amended Claim 1, their teachings even combined do not render the multi-layer printed wiring board recited in Claim 1 obvious. Londa is cited for teachings of conductive bumps and is not believed to teach or suggest the features absent from Sakamoto et al. and Jones et al. as noted above.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 3, 4, 6-8, 11, 12 and 18-20 depend directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 3, 4, 6-8, 11, 12 and 18-20 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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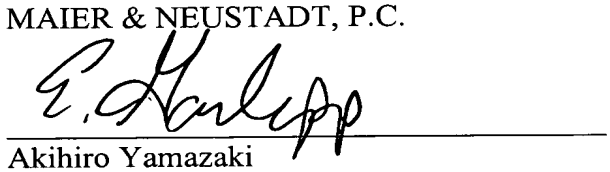

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